WHAT IS CLAIMED IS:

1. A semiconductor apparatus comprising a semiconductor device, an electrically insulating layer formed on said semiconductor device, an external connection terminal formed on said electrically insulating layer, and a wiring formed on said electrically insulating layer and provided for electrically connecting said external connection terminal to a circuit electrode of said semiconductor device, wherein at least one pair of opposite inclined portions of said electrically insulating layer are different in inclination angle from each other.

2. A semiconductor apparatus according to Claim 1, wherein said wiring is formed on one of said opposite inclined portions which is smaller in inclination angle than the other of said opposite inclined portions of said stress relaxation layer.

3. A semiconductor apparatus according to Claim 1, wherein said one inclined portion which is smaller in inclination angle has an inclination in a range of from about 5% to about 30% with respect to a surface of said semiconductor device.

4. A semiconductor apparatus according to Claim 1, wherein said electrically insulating layer contains particles.

5. A semiconductor apparatus according to Claim 1, wherein said electrically insulating layer has a thickness of about 35 μm to 150 μm.

6. A semiconductor apparatus according to any one of Claims 1 through 5, wherein said electrically insulating layer is formed by printing with use of a mask.

7. A method for producing a semiconductor apparatus, comprising:

a first step of forming a first electrically insulating layer on a wafer by printing with use of a mask so that said first electrically insulating layer is formed to extend over first and second semiconductor devices;

a second step of removing a portion which is a part of said first electrically insulating layer and which is located on a region between said first and second semiconductor devices; and

a third step of dicing said wafer.

8. A method for producing a semiconductor apparatus according to Claim 7, further comprising a fifth step of forming an external connection terminal on said first electrically insulating layer.

9. A method for producing a semiconductor apparatus, comprising:

a first step of forming a first electrically insulating layer on a wafer by printing with use of a mask so that said first electrically insulating layer is formed to extend over first and second semiconductor devices;

a second step of forming wiring on said first

electrically insulating layer;

a third step of removing a portion which is a part of said first electrically insulating layer and which is located on a region between said first and second semiconductor devices;

a fourth step of forming an external connection terminal on said first electrically insulating layer; and

a fifth step of dicing said wafer.

10. A method for producing a semiconductor apparatus according to Claim 9, further comprising a step of covering said first electrically insulating layer and said wiring with a second electrically insulating layer, said step being provided between said third and fourth steps.

11. A method for producing a semiconductor apparatus according to Claim 7 or 9, wherein a part of said first electrically insulating layer is removed by laser processing or mechanical processing.

12. A method for producing a semiconductor apparatus according to Claim 7 or 9, wherein said first electrically insulating layer is cut by a first cutter whereas said wafer is cut by a second cutter different from said first cutter.

13. A method for producing a semiconductor apparatus according to Claim 7 or 9, wherein said first electrically insulating layer is formed on said wafer so as to extend over four semiconductor devices which

are adjacent to each other.

14. A method for producing a semiconductor apparatus according to Claim 7 or 9, wherein said first electrically insulating layer is formed on said wafer so as to extend over two adjacent rows of semiconductor devices.

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